Based on this equation, it may be appreciated that increasing the load capacitance per unit length (C.sub.d) will result in decreasing values for the loaded impedance (Z'). Unfortunately, in backplane architectures, the buses are relatively short with each load device being separated by a relatively short distance. Since each load device adds capacitance to the bus, there is a tendency for backplane architectures to have relatively high values for load capacitance per unit length (C.sub.d). The result is that these architectures may be characterized by low intrinsic low values for impedance (Z'). Low values for impedance (Z') results in a slow propagation speed for signals within the bus. This degrades the performance of the bus, making it more prone to operational errors and electrical noise.

To overcome the degrading effects of decreasing impedance, designers have been faced with a difficult compromise. One possible solution is to increase the length of the bus included in backplane architectures. Typically this is achieved by increasing the effective distance that each signal must travel between adjacent intelligent peripheral devices. Unfortunately, this requires that the size of the backplane be increased or that each signal path be routed in a tortuous pattern between adjacent load devices. The use of a tortuous pattern increases the difficulty of routing the signal paths within the backplane and may require that additional signals layers be added to the backplane. In either case, the cost of the backplane can be increased significantly. Another possible solution is to decrease the clock speed of the bus. Of course, this negatively impacts the performance of the bus, thereby making this solution generally unacceptable.

In addition to the problems discussed above, using RAMBUS technology, current computer data speeds may operate at 800 mega-transfers per second. As a result, the edge rates of the data pulses are on the order of 200 picoseconds or 0.2 nanoseconds. For high speed data ASIC comparisons distortions may occur due to reflections of the data signal from the terminating end of the data signal path. This path may include the path through the silicon itself. Further the silicon path also has parasitic load that must be dealt with.

At these very high speeds (edge rates) the effect of otherwise small reactive components attached to electrical interconnects can have a very detrimental effect. The high speed edge rates of the Rambus-generated signals (e.g., in the Alpha EV7 that uses Rambus signals extensively) would cause significant signal reflections off of parasitic load points such as PWB routing vias or connector pins. Also, the transmission line electrical discontinuities caused by these physical discontinuities (like vias and connector pin metallization) would cause a noise margin reduction of these signals and possible logical failures.

Therefore there is now a need for a high speed bus or signal transmission line that has acceptable electrical signal impedance characteristics and operates at acceptable clock speeds.

SUMMARY OF THE INVENTION

The present invention addresses the aforementioned and related problems that are associated with a parasitic element. Since a discontinuity, such as a via, in a signal transmission line can introduce the parasitic element which affects the signal transmission, the present invention provides a method and system directed to counteracting that transmission line parasitic element discontinuity.

More specifically, in accordance with the purpose of the present invention, as embodied and broadly described herein, the system includes signal transmission line and a correction transmission line. The correction transmission line includes, based on the characteristics of the parasitic element, an inductance or a capacitance. The correction transmission line is positioned in the signal transmission line before or after the parasitic element.

In further accordance with the purpose of the present invention, as embodied and broadly described herein, one method includes determining a value of a parasitic element, be it a capacitive or an inductive parasitic element, that exists at a portion of a signal transmission line which has an impedance. This method also includes calculating a delay associated with a correction impedance of a correction transmission line that, based at least in part on the parasitic element value and the correction impedance of the correction transmission line, is operative to increase the signal transmission line impedance if the parasitic element is capacitive and to decrease the signal transmission line impedance if the parasitic element is inductive. This method further includes adding the correction transmission line to the portion of the signal transmission line at which the parasitic element exists.